

## Delay element

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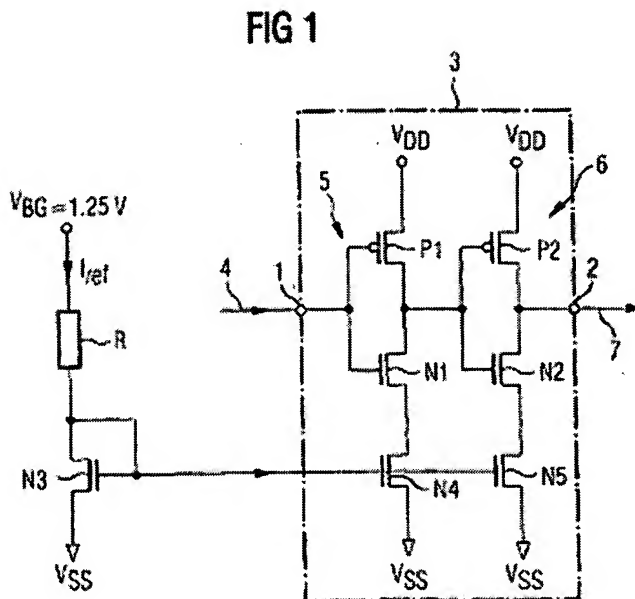
**Cited documents:**

US6034557  
US5841296  
US4932053  
US4295041  
US5544120  
US5250914  
US5459423  
EP0813303  
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## Abstract of EP1187331

The device has at least one electronic switch (5,6), to whose input (1) an input signal is applied and at whose output (2) an output signal appears, and a current limiting device (N4,N5), which limits the current consumption of the switch (es), whereby the switching time is extended by limiting the current consumption of the switch(es). The current limiting circuit is controlled by a current mirror. Independent claims are also included for the following: a memory controller with a delay line.



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